

## ABSTRACT OF THE DISCLOSURE

5 A source electrode  $V_{dd}$  is formed in a region between a field PMOS 1 and a field PMOS 2 as high side switches of a latch circuit. This latch circuit is utilized in the state where a lower side of one of the two high side switches is completely depleted. Field PMOS 1 and field PMOS 2 share a  $P^+$ -type impurity diffusion region, an  $N^+$ -type impurity diffusion region and a  $P^+$ -type impurity diffusion region, which are connected to source electrode  $V_{dd}$ . It is therefore possible to provide a semiconductor device capable of  
10 reducing the area thereof in the direction parallel to the main surface of a semiconductor substrate.